Claims

We claim:

1. A vector graphics circuit for rendering vector and bitmap graphics objects to a final image, the vector graphics circuit comprising:

a. an input display list means for receiving an input stream of data;

b. a sorting hardware circuit for optimizing the scan conversion algorithm;

c. a Bézier hardware circuit for vector curve subdivision;

d. an antialiasing hardware circuit for calculating sub-pixel values;

e. a color hardware circuit for reordering and for optimizing the access to a plurality of bitmaps and mathematical tables inside the display list memory;

f. a dump buffer hardware circuit, using a memory, which composes the vector graphics objects in a final pixel bitmap.

2. A vector graphics circuit according to claim 1 wherein the input display list means is arranged to include a quadratic or cubic Bézier edge data list.

3. A vector graphics circuit according to claim 2 wherein the input display list means is arranged to include a color data list.

4. A vector graphics circuit according to claim 3 wherein the input display list means is arranged to include a color rump data list.

5. A vector graphics circuit according to claim 3 wherein the input display list means is arranged to include a pattern or bitmap data list.

6. A vector graphics circuit according to claim 1 wherein the sorting hardware circuit comprises:

a. an active edge processor subunit that stores the edges of a current scan line inside an active edge table with increasing X, the active edge table comprises a dual port memory, where two alternating ping-pong buffers are stored;

b. a free active edge stack acting as a LIFO stack, to generate the address of the active edge table.

7. A vector graphics circuit according to claim 1 wherein a Bézier hardware circuit store a series of segments inside an dual port memory comprising:

a. a subdivided Bézier parameter unit, comprising three couples of X and Y adders/divide by two, plus a delay element;

b. a De Casteljau subdivision unit;

c. a Bézier subdivision tree address unit that generates the address locations of the Bézier segments inside a dual port memory.

8. A vector graphics circuit according to claim 1 wherein the antialiasing hardware circuit computes the number of sub-pixels present in a N = i*4 real pixels per clock, to obtained the weight factor used for a scan-converted row.

9. A vector graphics circuit according to claim 1 wherein the color hardware circuit includes:

a. a color generator sub unit that outputs a solid or a processed color when a linear gradient, a radial gradient a tiled bitmap or a clipped bitmap are associated with the active edge;

b. a color composer sub unit that uses the weight factor to process the color from the color generator and store the result in to a dump buffer.

10. A vector graphics circuit according to claim 1 wherein the buffer hardware circuit stores a pixel region into a buffer, where all the objects are composed, comprising:

a. a fixed single line dump buffer memory that stores the color pixels processed by an antialiasing and transparence factors;

b. a store buffer memory that stores the color pixel value using the following algorithm:

i. Read the background pixel from the store buffer memory, multiply it by the complementary of the transparence (1 - alpha), obtained from the dump buffer, and add it with the red, green, blue values again from the dump buffer.

ii. The result is written again inside the store buffer.

12. A vector graphics circuit according to claim 1 wherein a Bézier hardware circuit store a series of segments inside an dual port memory comprising:

a subdivided Bézier parameter unit, comprising three couples of X and Y adders/divide by two, plus a delay element.

13. A vector graphics circuit according to claim 1 wherein a Bézier hardware circuit store a series of segments inside an dual port memory comprising:

a De Casteljau subdivision unit.

14. A vector graphics circuit according to claim 1 wherein a Bézier hardware circuit store a series of

segments inside an dual port memory comprising:

a Bézier subdivision tree address unit that generates the address locations of the Bézier segments inside a dual port memory;

15. A vector graphics circuit for rendering vector and bitmap graphics objects to a final image, the vector graphics circuit comprising:

a. an input display list means for receiving an input stream of data;

b. a sorting hardware circuit for optimizing the scan conversion algorithm;

c. a Bézier hardware circuit for vector curve subdivision;

d. an antialiasing hardware circuit for calculating sub-pixel values;

e. a color hardware circuit for reordering and for optimizing the access to a plurality of bitmaps and mathematical tables inside the display list memory;

f. a dump buffer hardware circuit, using a memory, which composes the vector graphics objects in a final pixel bitmap,

wherein the input display list means is arranged to include a quadratic or cubic Bézier edge data list,

wherein the input display list means is arranged to include a color data list,

wherein the input display list means is arranged to include a color rump data list,

wherein the input display list means is arranged to include a pattern or bitmap data list,

wherein the sorting hardware circuit comprises:

a. an active edge processor subunit that stores the edges of a current scan line inside an active edge table with increasing X,

the active edge table comprising a dual port

memory, where two alternating ping-pong buffers are stored;

b. a free active edge stack acting as a LIFO stack, to generate the address of the active edge table,

wherein a Bézier hardware circuit store a series of segments inside an dual port memory comprising:

a. a subdivided Bézier parameter unit, comprising three couples of X and Y adders/divide by two, plus a delay element;

b. a De Casteljau subdivision unit;

c. a Bézier subdivision tree address unit that generates the address locations of the Bézier segments inside a dual port memory,

wherein the antialiasing hardware circuit computes the number of sub-pixels present in a N = i*4 real pixels per clock, to obtained the weight factor used for a scan-converted row,

wherein the color hardware circuit includes:

a. a color generator sub unit that outputs a solid or a processed color when a linear gradient, a radial gradient a tiled bitmap or a clipped bitmap are associated with the active edge;

b. a color composer sub unit that uses the weight factor to process the color from the color generator and store the result in to a dump buffer,

wherein the buffer hardware circuit stores a pixel region into a buffer, where all the objects are composed, comprising:

a. a fixed single line dump buffer memory that stores the color pixels processed by an antialiasing and transparence factors;

b. a store buffer memory that stores the color pixel value using the following algorithm:

i. Read the background pixel from the store

buffer memory, multiply it by the complementary of the transparence (1 - alpha), obtained from the dump buffer, and add it with the red, green, blue values again from the dump buffer.

ii. The result is written again inside the store buffer.